

PCT

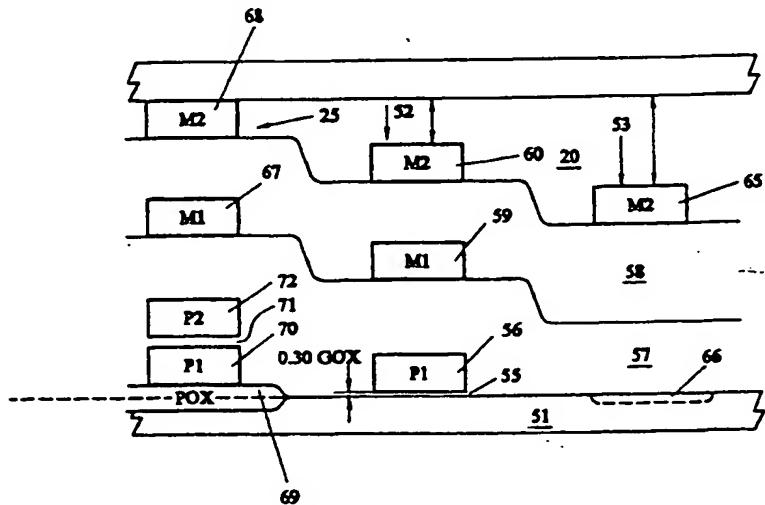
WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ :	A1	(11) International Publication Number:	WO 00/37996
G02F 1/1339, 1/1362		(43) International Publication Date:	29 Jun 2000 (29.06.00)
<p>(21) International Application Number: PCT/GB99/04282</p> <p>(22) International Filing Date: 16 December 1999 (16.12.99)</p> <p>(30) Priority Data: 9827900.3 19 December 1998 (19.12.98) GB</p> <p>(71) Applicant (for all designated States except US): THE SECRETARY OF STATE FOR DEFENCE [GB/GB]; Defence Research and Evaluation Agency, Ively Road, Farnborough, Hampshire GU14 0LX (GB).</p> <p>(72) Inventors; and</p> <p>(75) Inventors/Applicants (for US only): CROSSLAND, William, Alden [GB/GB]; University of Cambridge, Engineering Dept., Trumpington Street, Cambridge CB2 1PZ (GB). WILKINSON, Timothy, David [GB/GB]; University of Cambridge, Engineering Dept., Trumpington Street, Cambridge CB2 1PZ (GB). YU, Tat, Chi, B. [-]; - (**).</p> <p>(74) Agents: GODDARD, David, John; Harrison Goddard Foote, 1 Stockport Road, Marple, Stockport SK6 6BD (GB) et al.</p>		<p>(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published With international search report.</p>	

(54) Title: SPACERS FOR CELLS HAVING SPACED OPPPOSED SUBSTRATES



(57) Abstract

In an active semiconductor backplane for a liquid crystal spatial light modulator, spacers (25) which are distributed over the backplane extend above an array of electrical and/or electronic elements and comprise at least two layers essentially of the same material and occurring in the same order as is found in at least one of the electrical or electronic elements, such as an NMOS transistor (52). The latter is formed from a stack of layers on a silicon substrate (51) comprising polysilicon (56), continuous silicon oxide (57) modified to include gate oxide GOX (55), metallic gate electrode (59), continuous silicon oxide (58) and a metallic drain electrode (60) which is coupled to a spaced mirror electrode over the layer (58). Likewise, spacer (25) comprises the layers (57 and 58) with metallic (67, 68) deposited simultaneously with electrodes (59, 60). The foot of layer (57) is differently modified to include field oxide layer (69) and polysilicon layers (70, 72) spaced by thin oxide (71). Spacers (25) are located regularly within the array of transistors (25)/mirrors (65) and also about the array.